LISTING OF CLAIMS

1. (Currently Amended) A CMOS imager, comprising:

a photoconversion device; and

a first transistor having a gate with a first side and a second side opposite said first side, said gate being associated with said photoconversion device at [[a]] said first side of said ~~first transistor~~ gate, said first transistor also having a single active area extension region ~~on a~~ associated with said second side of said ~~transistor opposite said first side~~ gate and a halo implant region below said single active area extension region.

2. (Original) The CMOS imager of claim 1, wherein said first transistor is a reset transistor in electrical communication with said photoconversion device.

3. (Original) The CMOS imager of claim 1, wherein said first transistor is a transfer transistor in electrical communication with said photoconversion device.

4. (Original) The CMOS imager of claim 1, wherein said first transistor has an underlying channel region, said channel region having a threshold voltage adjustment implant.

5. (Original) The CMOS imager of claim 1, wherein said first transistor has a gate length which is increased relative to other transistors in electrical communication with said photoconversion device.

6. (Currently Amended) The CMOS imager of claim 1, ~~comprising a halo implant region below said single active area extension region,~~ wherein said halo implant region ~~extending~~ extends partially below [[a]] the gate of said first transistor.

7. (Original) The CMOS imager of claim 1, wherein said photoconversion device is one of a photodiode, a photogate, or a photoconductor.

8. (Currently Amended) The CMOS imager of claim [[6]] 1, wherein said single active area extension region and said halo implant region are laterally spaced away from [[a]] the gate of said first transistor by a portion of a substrate supporting said first transistor.

9. (Original) The CMOS imager of claim 1, wherein said photoconversion device is part of a four transistor pixel circuit comprising a transfer transistor as said first transistor, a reset transistor, a source follower transistor, and a row select transistor.

10. (Original) The CMOS imager of claim 9, wherein at least one of said reset transistor and said source follower transistor have a single active area extension region.

11. (Withdrawn) The CMOS imager of claim 1, wherein said photoconversion device is part of a three transistor circuit comprising a reset transistor as said first transistor, a source follower transistor, and a row select transistor.

12. (Withdrawn) The CMOS imager of claim 11, wherein said source follower transistor has a single active area extension region.

13. (Original) The CMOS imager of claim 1, wherein said active area extension region of said first transistor has a dopant concentration of about 1×10^{12} to about 3×10^{13} ions/cm^2.

14. (Original) The CMOS imager of claim 1, wherein said first transistor has a single insulating spacer, said spacer positioned on said second side of said transistor.

15. (Currently Amended) A pixel sensor cell, comprising:

a semiconductor substrate;

a transfer transistor over said substrate, said transfer transistor having a single active area extension region located on a first side of said transfer transistor;

a photosensor in electrical communication with said transfer transistor, said photosensor being within said substrate on a second side of said transfer transistor which is opposite to said first side;

a reset transistor gate over said substrate and spaced apart from said transfer transistor; and

a floating diffusion region on the first side of said transfer transistor and adjacent said reset transistor gate, said floating diffusion region being in electrical communication with said active area extension region and having a halo implant region.

16. (Original) The pixel sensor cell of claim 15, wherein said transfer transistor has an underlying channel region, said channel region having a threshold voltage adjustment implant.

17. (Original) The pixel sensor cell of claim 15, wherein said transfer transistor has a gate length which is increased relative to other transistor gates in electrical communication with said photosensor.

18. (Original) The pixel sensor cell of claim 15, wherein said reset transistor comprises two active area extension regions as lightly doped drains on opposite sides of said reset transistor gate.

19. (Original) The pixel sensor cell of claim 15, wherein said reset transistor comprises a single active area extension region on a side opposite said floating diffusion region.

20. (Original) The pixel sensor cell of claim 15, further comprising at least a source follower transistor and a row select transistor.

21. (Original) A pixel sensor cell, comprising:

a semiconductor substrate;

a reset transistor over said substrate;

a photosensor in electrical communication with said reset transistor, said photosensor being within said substrate on a first side of said reset transistor;

a single active area extension region in said substrate adjacent to said reset transistor, said single active area extension region being on a side of said reset transistor which is opposite to said first side; and

a halo implant region in said substrate below said single active area extension region.

22. (Original) The pixel sensor cell of claim 21, wherein said reset transistor has an underlying channel region, said channel region having a threshold voltage adjustment implant.

23. (Withdrawn) The pixel sensor cell of claim 21, wherein said reset transistor has a gate length which is increased relative to other transistor gates in electrical communication with said photosensor.

24. (Original) The pixel sensor cell of claim 21, wherein said photosensor and said reset transistor are part of a transistor pixel circuit that further comprises a source follower transistor and a row select transistor.

25. (Original) The pixel sensor cell of claim 22, wherein said single active area extension region of said reset transistor is a lightly doped drain.

26. (Currently Amended) An image sensor, comprising:

a semiconductor substrate;

a reset transistor over said substrate;

a floating diffusion region in said substrate and in electrical communication with said reset transistor at a first side of said reset transistor;

a single active area extension region in said substrate adjacent to said reset transistor, said single active area extension region being on a second side of said reset transistor which is opposite to said first side; and

a halo implant region in said substrate below said single active area extension region.

27. (Original) The image sensor of claim 26, wherein the image sensor is a CMOS imager.

28. (Original) The image sensor of claim 27, further comprising a photodiode in electrical contact with said reset transistor, said photodiode being within said substrate on said first side of said reset transistor.

29. (Original) The image sensor of claim 27, wherein said floating diffusion region is located within a sensor array.

30. (Withdrawn) The image sensor of claim 26, wherein the image sensor is a CCD imager.

31. (Original) The image sensor of claim 29, wherein said floating diffusion region is located outside a sensory array.

32. (Currently Amended) An imager device, comprising:

an image processor; and

a pixel array for supplying signals to said image processor, at least one pixel of said array comprising:

a photoconversion device, and

a first transistor gate associated with said photoconversion device at a first side of said transistor gate, said transistor gate having a single lightly doped drain on a second side of said transistor gate opposite said first side, an underlying channel region having a threshold voltage adjustment implant, a halo implant below said lightly doped drain, and said gate also having a length which is increased relative to other transistor gates of said pixel.

33. (Original) The imager device of claim 32, wherein said first transistor gate is of a reset transistor in electrical communication with said photoconversion device.

34. (Original) The imager device of claim 32, wherein said first transistor gate is of a transfer transistor in electrical communication with said photoconversion device.

35. (Cancelled).

36. (Cancelled).

37. (Original) The imager device of claim 32, wherein said photoconversion device is a photodiode.

38. (Currently Amended) ~~A semiconductor~~ An integrated circuit, comprising a transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region on a side of said transistor opposite from said photodiode and a halo implant below said single active area extension region.

39. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 38, further comprising a threshold voltage adjustment implant below a gate of said transistor.

40. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 38, wherein said transistor has a gate length which is increased relative to any transistor gate length of other transistors of a same pixel.

41. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 38, further comprising a source/drain region adjacent to said active area extension region, said active area extension region and said source/drain region being spaced

away from a gate of said transistor by a portion of a substrate supporting said transistor.

42. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 38, further comprising an insulating layer over said transistor and said photodiode, said insulating layer extending to a floating diffusion region adjacent to said active area extension region.

43. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 38, wherein said transistor and said photodiode are part of a CMOS imager pixel.

44. (Withdrawn) The ~~semiconductor transistor~~ integrated circuit of claim 38, wherein said transistor and said photodiode are part of a CCD imager.

45. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 38, wherein said transistor is part of a pixel having at least two other transistors in electrical communication with said photodiode.

46. (Currently Amended) A ~~semiconductor~~ pixel cell, comprising a transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region and halo implant region on a opposite side of said transistor from said photodiode, said transistor also having a gate length which is increased relative to any other transistor gate length of transistors of a same pixel.

47. (Cancelled).

48. (Currently Amended) The ~~semiconductor transistor~~ pixel cell of claim [[47]] 46, comprising a threshold voltage adjustment implant below a gate of said transistor.

49. (Currently Amended) The ~~semiconductor transistor~~ pixel cell of claim [[47]] 46, comprising a source/drain region adjacent to said active area extension region, said active area extension region and said source/drain region being spaced away from a gate of said transistor by a portion of a substrate supporting said transistor ~~by a portion of a substrate supporting said transistor~~.

50. (Currently Amended) ~~A semiconductor~~ An integrated circuit, comprising a transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region on a opposite side of said transistor from said photodiode and a halo implant and a source/drain region adjacent ~~to~~ said active area extension region, said active area extension region, said halo implant, and said source/drain region being spaced away from a gate of said transistor.

51. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 50, further comprising a threshold voltage adjustment implant below a gate of said transistor.

52. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 51, wherein said transistor and photodiode are part of a pixel cell and said transistor has a gate length which is increased relative to any other transistor gate length of transistors of ~~a same~~ said pixel cell.

53-84. (Cancelled).

85. (Currently Amended) ~~A semiconductor~~ An integrated circuit, comprising a transistor comprising a channel region between a higher voltage side and a lower voltage side, and a single active area extension region with a halo implant at said higher voltage side of said channel~~, said transistor being associated with circuitry of a photoimaging circuit~~.

86. (Currently Amended) The ~~semiconductor transistors~~ integrated circuit of claim 85, wherein said transistor is part of a pixel.

87. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 85, wherein said transistor has a gate length which is increased relative to any transistor gate length of other transistors of a same photoimager circuit.

88. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 85, further comprising a threshold voltage adjustment implant below a gate of said transistor.

89. (Currently Amended) The ~~semiconductor transistor~~ integrated circuit of claim 85, wherein said transistor is associated with a photodiode of a CMOS imager pixel.

90. (Withdrawn) The ~~semiconductor transistor~~ integrated circuit of claim 85, wherein said transistor is part of a CCD imager.

91. (Withdrawn) A CCD imager comprising at least one transistor gate with a single active area extension region at a higher voltage side of said at least one transistor gate.

92. (Withdrawn) The CCD imager of claim 91, wherein said at least one transistor gate is of a reset transistor.

93. (Withdrawn) The CCD imager of claim 91, wherein said at least one transistor gate is of a source follower transistor.